AMENDMENTS TO THE CLAIMS

Please amend the claims follows:

1. (Currently Amended) A source driving circuit for a liquid crystal display (LCD) for driving an LCD panel in response to digital image signals, the source driving circuit comprising:

~~first and second~~a multiplexing-latch circuits~~, wherein each of the multiplexing-latch circuits is~~ adapted to ~~latch a dynamically selected~~ and latch and output one of a first and second digital image signals ~~dynamically selected~~ in response to first and second selection signals ~~and to output one of the latched first and second digital image signals~~,

wherein the multiplexing latch circuit comprises a plurality of inverters and transmission gates configured to form a first latch including a gate unit, and a second latch,

wherein the gate unit includes first and second transmission gates,

wherein the first latch includes the gate unit, and first and second inverters,

wherein the second latch includes third and fourth inverters,

wherein the output node of the first latch is connected to the input node of the third inverter through the fourth transmission gate, and the first and second transmission gates are directly connected to the input node of the first inverter.

2. (Currently Amended) The source driving circuit of claim 1, further comprising:

a second multiplexing-latch circuit having the same internal structure as the first multiplexing-latch circuit;

a plurality of level shifters for increasing logic voltage levels of the latched digital image signal data received from the first and second multiplexing--latch circuits and outputting the levelshifted latched data;

a plurality of positive decoders, wherein each of the positive decoders is adapted to output a dynamically selected one of a plurality of positive reference voltages in response to

the latched data received from the plurality of level shifters, each of the positive reference voltages having different voltage levels and positive polarities;

a plurality of negative decoders, wherein each of the negative decoders is adapted to output a dynamically selected one of a plurality of negative reference voltages in response to the latched data received from the plurality of level shifters, the negative reference voltages having different voltage levels and negative polarities;

a plurality of multiplexor (MUX) circuits, wherein each of the MUX circuits is adapted to output a selected one of the positive and negative reference voltages as an analog image signal in response to a MUX selection signal~~;~~ and

a plurality of amplifiers adapted to increase the magnitude of electric current of the analog image signals output at the positive and negative reference voltages.

3. (Currently Amended) The source driving circuit of claim 2, further comprising a plurality of operatively connected pairs of first and second multiplexing-latch circuits, wherein the pairs are categorized into three groups, wherein each group is adapted to latch a predetermined pair of color signals selected from: R and G color signals B and R color signals, and G and B color signals~~.~~.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) The source driving circuit of claim 61, wherein the first selection signal is disabled when the second selection signal is enabled.

8. (Currently Amended) The source driving circuit of claim ~~6~~7, wherein the first and second selection signals are enabled or disabled in response to a polarity signal that is one of a plurality of control signals output from a control circuit.

9. (Currently Amended) A source driving circuit for a liquid crystal display (LCD) that drives an LCD panel in response to digital image signals, the source driving circuit comprising:

a plurality of pairs of first and second multiplexing-latch circuits, wherein each of the first and second multiplexing-latch circuits is adapted to select and latch and output ~~a dynamically selected~~ one of a first and second digital image signals ~~dynamically selected~~ in response to first and second selection signals ~~and to output one of the latched first and second digital image signals,~~

wherein each of the first and second multiplexing-latch circuits includes a master latch circuit and a corresponding slave latch circuit and is configured to function as a master-slave latch adapted to select and latch one of a first and second digital image signals,

wherein the master latch circuit of each multiplexing-latch circuit includes a gate unit, a first inverter and a second inverter,

wherein the gate unit includes first and second transmission gates, wherein each of the first and second transmission gates is connected to the input node of the first inverter of the master latch circuit and is configured to pass a predetermined one of the first and second digital image signals to the input node of the first inverter of the master latch circuit, in response to one of the first and second selection signals being enabled.~~,~~

10. (Currently Amended) The source driving circuit of claim 9, wherein the output node of the second inverter of the master latch circuit is the output node of the master latch circuit.

~~each of the first and second multiplexing-latch circuits includes a master latch circuit and a slave latch circuit.~~

11. (Currently Amended) The source driving circuit of claim 10, wherein the ~~master latch circuit and a~~ slave latch circuit of each multiplexing-latch circuit includes ~~a latch unit~~two inverters; and wherein

~~a predetermined one of the master latch circuit and a slave latch circuit of each multiplexing latch circuit includes a gate unit, wherein the gate unit includes first and second transmission gates, wherein each of the transmission first and second transmission gates is adapted to pass a predetermined one of the first and second digital image signals to the latch unit of the same latch circuit in response to one of the first and second selection signals being enabled.~~

12. (Canceled)

13. (Original) The source driving circuit of claim 12, wherein the first selection signal is disabled when the second selection signal is enabled, and the second selection signal is disabled when the first selection signal is enabled.

14. (Currently Amended) The source driving circuit of claim 12, wherein

wherein the master latch circuit of each multiplexing-latch circuit further includes a third transmission gate wherein the third transmission gate is a feedback transmission gate connected between the output node of the second inverter of the master latch circuit and the input node of the first inverter of the master latch circuit,

wherein the second inverter of the master latch circuit is ~~each of the master latch circuit and the slave latch circuit of each multiplexing latch includes a first inverter and a~~ feedback inverter, wherein the input node of the ~~feedback~~ second inverter is connected directly to the output node of the first inverter, and the output node of the ~~feedback~~ second inverter is connected, through third transmission gate, to the input node of the first inverter.

15. (Currently Amended) The source driving circuit of claim 14, wherein each of the first and second transmission gates is adapted to pass a predetermined one of the first and second digital image signals directly to the input node of the first inverter of ~~the latch unit of the~~ master latch circuit in response to one of the first and second selection signals being enabled.

16. (Currently Amended) The source driving circuit of claim 15, wherein wherein each of the first and second multiplexing-latch circuits includes no more than five transmission gates and no more than four inverters~~the master latch circuit of each multiplexing latch further includes a third transmission gate operatively connected to and between the input of the first inverter and the output of the master latch circuit~~.

17. (Currently Amended) The source driving circuit of claim 16, wherein each of the first and second multiplexing-latch circuits includes no more than 18 field effect transistors~~the third transmission gate is operatively connected to and between the input of the first inverter and the output of the feedback inverter~~.

18. (Currently Amended) An article of manufacture comprising:

a master-slave latch circuit adapted to dynamically select and to latch one of a first and second externally supplied independent voltage signals and to output one of the first and second voltage signals,

~~,~~wherein the master-slave latch circuit includes a master latch circuit and a corresponding slave latch circuit,

wherein the master latch circuit includes a gate unit, a first inverter and a second inverter,

wherein the gate unit includes first and second transmission gates, each of the first and second transmission gates is connected to the input node of the first inverter of the master latch circuit and is configured to pass a predetermined one of the first and second

digital image signals to the input node of the first inverter of the master latch circuit, in response to one of the first and second selection signals being enabled.

19. (New) The article of claim 18, wherein

the master-slave latch circuit includes no more than five transmission gates and no more than four inverters.

20. (New) The source driving circuit of claim 1, wherein

each of the inverters comprises two complementary field-effect transistors (FETs) connected in series and wherein each of the transmission gates comprises two complementary FETs connected in parallel.